ABSTRACT OF THE DISCLOSURE

A PLL circuit may include a memory for storing a control voltage and a processor for loading a control voltage, which corresponds to a changed channel, from the memory when a system channel is changed, and providing the control voltage to a Voltage Control Oscillator (VCO). Whenever a system changes a channel, a control voltage of a pertinent channel frequency that has been stored in the memory may be used as an initial value of a control voltage provided to the VCO 50 so that a time (i.e., a lock time) to perform a phase lock looping may be remarkably reduced. This may improve a processing speed of various communication equipments and their performance.